Abstracts

A novel cold-FET method for determining extrinsic capacitances using a capacitive transmission line model

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A novel cold-FET method using a capacitive transmission line (CTL) model to extract extrinsic capacitances for the small-signal equivalent circuit of field-effect transistors (FET's) is proposed. The extrinsic gate capacitance (C/sub pg/) and drain capacitance (C/sub pd/) of the FET's are extracted on the basis of the distributed CTL model and ABCD matrix representation for the depletion region beneath gate under the pinched-off cold-FET condition. The extraction method proposed is applied to obtain the small-signal equivalent circuit model for the FET's. The simulated S parameters using the CTL model exhibit great agreement with the measured S parameters.

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